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A Multiple Window Demonstration of the Operation of PN Diodes Using DEVSIM*

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The one-dimensional device simulator DEVSIM is a useful tool for the multiple window demonstration of the operation of forward- and reverse-biased PN diodes. The graphical user interface allows for correlating the output I–V and C–V characteristics with internal device properties such as the spatial distributions of the electric potential, the electric field, the free carriers, their mobility and velocity, the band gap diagram and other quantities which are not ready for direct measurement. In combination with process simulation, the influence of variations in the technological process conditions on the output electrical characteristics can be analysed.

1. INTRODUCTION

MODELLING and numerical simulation play an increasingly important role in the development of modern technologies. By means of simulation, microscopic physical phenomena and effects occurring on very small length scales and on very short time scales can be visualised in macroscopic dimensions and, thus, made perceivable to our eyes and mind. Highly sophisticated physical models are implemented in the simulation tools, providing realistic results with good agreement between the real and the virtual (simulated) world. Hence, simulation is useful not only for qualitative understanding, but even for the quantitative predictive analysis of the properties of new semiconductor structures and devices.

Physical electronics is a typical example where modelling and simulation have proved to be very powerful and effective tools for research and development, including their use for education and training. Here, the calculation of electrical quantities and characteristics of semiconductor structures implies the numerical solution of the basic semiconductor equations, i.e. the coupled set of Poisson equations, the continuity equations for carrier flow and the constitutive current relations (drift–diffusion equations). Physical models, which include the dependence on temperature, doping concentration and electric field, are implemented in the numerical solution procedures. There exist various two- and three-dimensional simulators such as PISCES and DAVINCI distributed by American vendors, SIMUL developed at the Swiss Federal Institute of Technology Zurich, and MINIMOS and BAMBI developed by the Technical University Vienna, which feature highly advanced models and are applicable even to very complex device structures. However, the visualisation and interpretation of the simulated results are non-trivial problems and require much expertise from the user. Therefore, there is still a need for a reliable one-dimensional simulator with a flexible and user-friendly graphical support, in particular with a view to training and educational purposes.

2. DESCRIPTION OF OUR DEVICE SIMULATOR

Running the device simulator DEVSIM [1] requires an AT-compatible PC (e.g. with 386 + 387 or 486 processor) operated under the Windows surface, thereby providing a flexible and easy-to-use graphical environment [2]. The program code is written in Turbo Pascal and has a modular architecture. Therefore, new and more complex physical models may easily be added to the program or substituted for the old ones.

On parallel-opened windows, several quantities are simultaneously displayed, thus allowing the immediate correlation of the electrical characteristics with internal quantities such as doping profile and other structural properties. Internal dynamic variables within the structure considered as, for example, the electrostatic potential and the electric field, the distributions of the free carriers, their mobilities and velocities, and other physical properties which are not ready for direct measurement, are simultaneously visualised on the screen. So simulation leads to unique insight into the internal semiconductor structures. DEVSIM is based on

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advanced physical models [3, 4] where the physical parameters may be adjusted by the user in order to validate the models for a given technological process. Emphasis is laid on a judicious treatment of metal–semiconductor junctions. So, for instance, a special boundary condition for Schottky contact [5] is implemented.

DEVSIM is very easy to use. An integrated on-line help function facilitates the operation of the simulator so that virtually anybody with a basic knowledge of personal computers will be familiar with the simulator after a short time. The impact of the DEVSIM on user knowledge is even stronger when it is used together with some one-dimensional process simulator which provide a doping profile of active impurities in the formatted data file (dimension in the first column, net doping in the second and total concentration of impurities in the third). The influence of technological data which characterise the device fabrication on the electrical output characteristics can be analysed.

3. EXAMPLE

The examples discussed in the figures illustrate the performance of DEVSIM and elucidate its advantages in training students in the field of physical electronics.

Figure 1 shows a typical example of the multiple-window visualisation of simulated results using the Windows surface. The calculated output electrical I–V and C–V characteristics can easily be cross-referenced to the doping profile, the free carrier concentration and the mobility and drift velocity of the free carriers in the interior of the device structure under analysis.

Let us first consider the case of a reverse biased pn-junction. We assume an epitaxial layer of n-type Si with a donor concentration $N_d = 10^{16}$, cm^{-3}, grown on a high conductivity substrate with $N_d = 10^{19}$ cm^{-3}. An abrupt pn-junction is formed by a boron diffusion with a surface concentration of $N_a = 10^{19}$ cm^{-3}. The lifetime of the free electrons and holes is set to $\tau_{n,p} = 10^{-6}$ s^{-1}.

Figure 2 shows the distribution of free carriers, net doping profile and electrostatic potential distribution in the equilibrium state (a) and in the state biased by the applied voltage (b). The value of built-in voltage as well as the thickness of a space charge region around the pn-junction can be determined. The changes in the thickness of the space charge region and in the free carrier concentrations due to the variation of the applied voltage may directly be correlated with the output I–V and C–V characteristic (Fig. 1). Also the influence of the doping profile on current density and capacitance can easily be analysed. To this end, it is advantageous to use the device simulator in combination with a suitable process simulator which generates the doping profile for the different technological process parameters used during sample preparation.

The dependence of the carrier mobility (as depicted in Fig. 1) on the impurity concentration and the electric field strength is displayed in Fig. 3. The high concentration of impurities at the left- and right-hand ends of the analysed structure is the cause of the low mobility encountered there (Fig. 3a), whereas the local minimum in mobility at the pn-interface is effected by the strong electric field in the space charge region (Fig. 3b) driving the free carriers up to saturation velocity in this region (cf. Fig. 1).

The effect of generation–recombination processes on the internal behaviour of the analysed structure is illustrated in Figs 4 and 5. The efficiency of the Shockley–Read–Hall generation–recombination processes is controlled by the lifetime of free electrons and holes. Figure 4a shows the electric potential and the free-carrier distributions inside the device structure at 40 V reverse voltage for a carrier lifetime of 10^{-6} s, while Fig. 4b shows the same quantities for a carrier lifetime of 10^{-8} s. The two orders of magnitude difference in lifetime translates into a two orders of magnitude difference in the carrier concentration in the space charge region. This, in turn, results in about two orders of magnitude higher current density in the structure with shorter lifetime (Fig. 5a), while the capacitance is almost the same (Fig. 5b).

The effect of the carrier lifetime on the operational behaviour of the device is also nicely demonstrated for forward bias. Figure 6 displays electric potential and free-carrier concentrations for the two above-mentioned lifetimes. Due to the higher recombination rate at the shorter lifetime, the diffusion length of the free carriers is lower for the diode with a lifetime of 10^{-8} s (Fig. 6b). This results in a significantly stronger decay of the minority carrier concentration at each side of the pn-junction when compared to the structure with a carrier lifetime of 10^{-6} s (Fig. 6a).

The energy band diagram and the splitting of the quasi-Fermi level in the forward-biased case are shown in Fig. 7. Again the influence of varying diffusion length caused by different lifetimes of the free carriers is clearly visible. For the shorter carrier lifetime, the diffusion length is shorter and, hence, the quasi-Fermi levels coincide over a considerable distance on the right-hand part of the diode (Fig 7b), while in the structure with the longer carrier lifetime the quasi-Fermi levels are different everywhere except for the contacts at the right- and left-hand boundaries, where they become equal in consequence of the boundary conditions imposed (Fig. 7a).

4. CONCLUSION

We have demonstrated the advantage of 'multiple-window display' or simulation results in the analysis of semiconductor devices, in particular with a view to educational purposes. With a

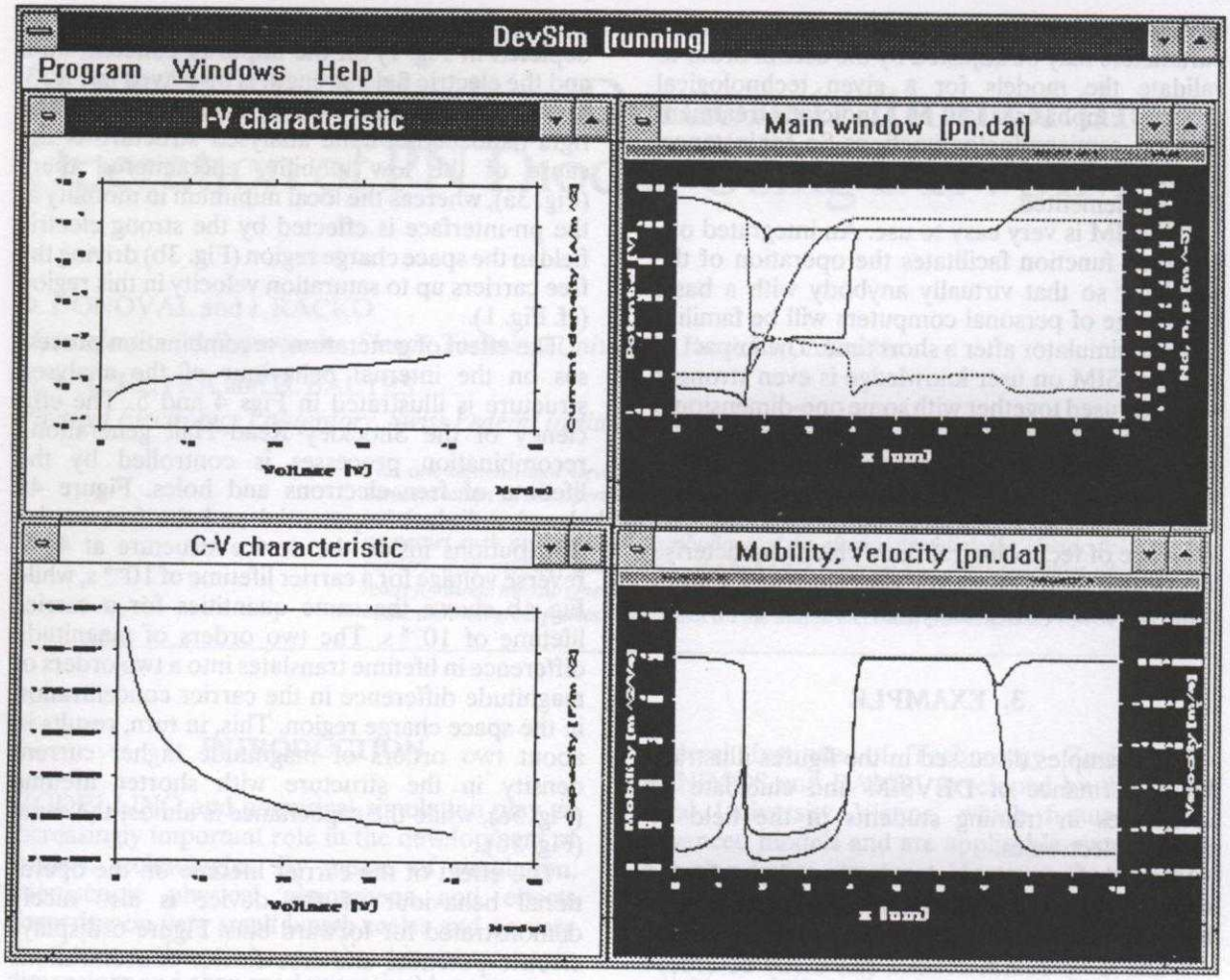

Fig. 1. Multiple-window display of simulation results computed by DEVSIM.

PIN diode as an illustrative example, it has been shown that Windows is a suitable graphical framework for cross-referencing the output electrical characteristics with the physical and structural properties in the interior of a semiconductor device. Coupling one-dimensional process simulation with DEVSIM allows us to use realistically modelled doping profiles and, thereby, to study the dependencies of the output I–V and C–V characteristics on the process parameters which control the fabrication steps.

After having obtained agreement between experiments and simulated results, modelling can provide valuable aid for design optimisation and the predictive analysis of novel semiconductor structures and their properties.

Furthermore, device simulation has proven to be an increasingly helpful technique in the education and training of microelectronics students. To this end, an easy-to-use, one-dimensional simulator with flexible and efficient graphical support as offered by DEVSIM may lend unique insight into the details of the device operation, thus enlarging the student's knowledge and expertise [6, 7].

DEVSIM has been successfully employed in the graduate courses of 'physical electronics' and 'physics of semiconductor structures' taught at the Microelectronics Department of the Slovak Technical University in Bratislava, the Physical Electronics Laboratory of the Swiss Federal Institute of Technology in Zurich, and it is also implemented at UMIST in Manchester, UK and at the Fachhochschule Munich, Germany.

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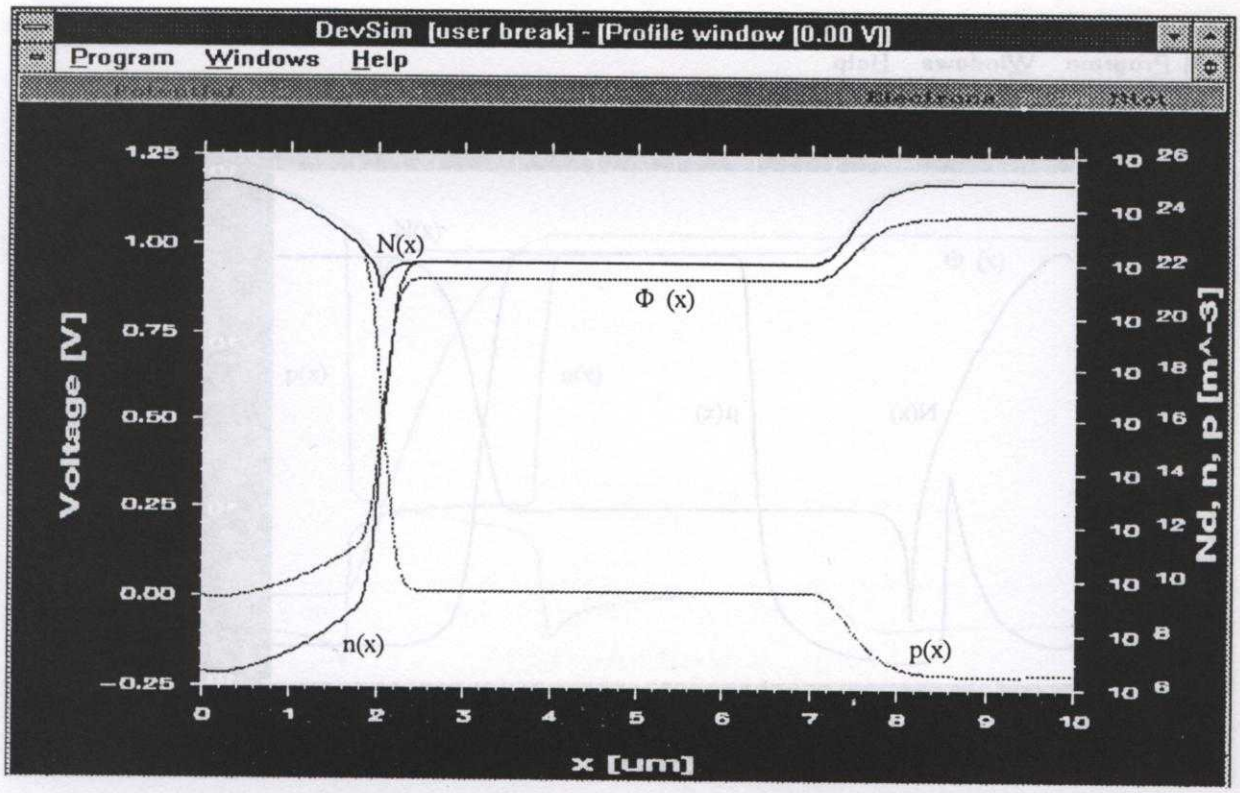

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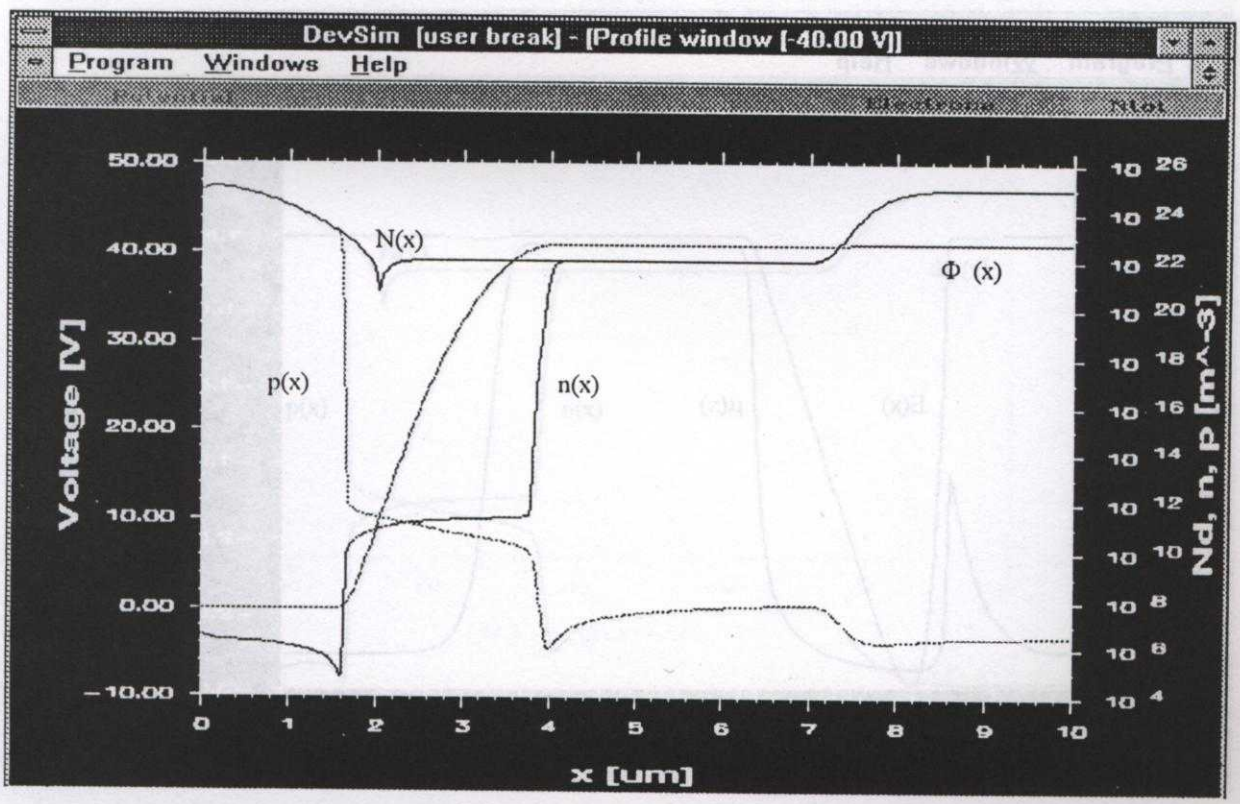
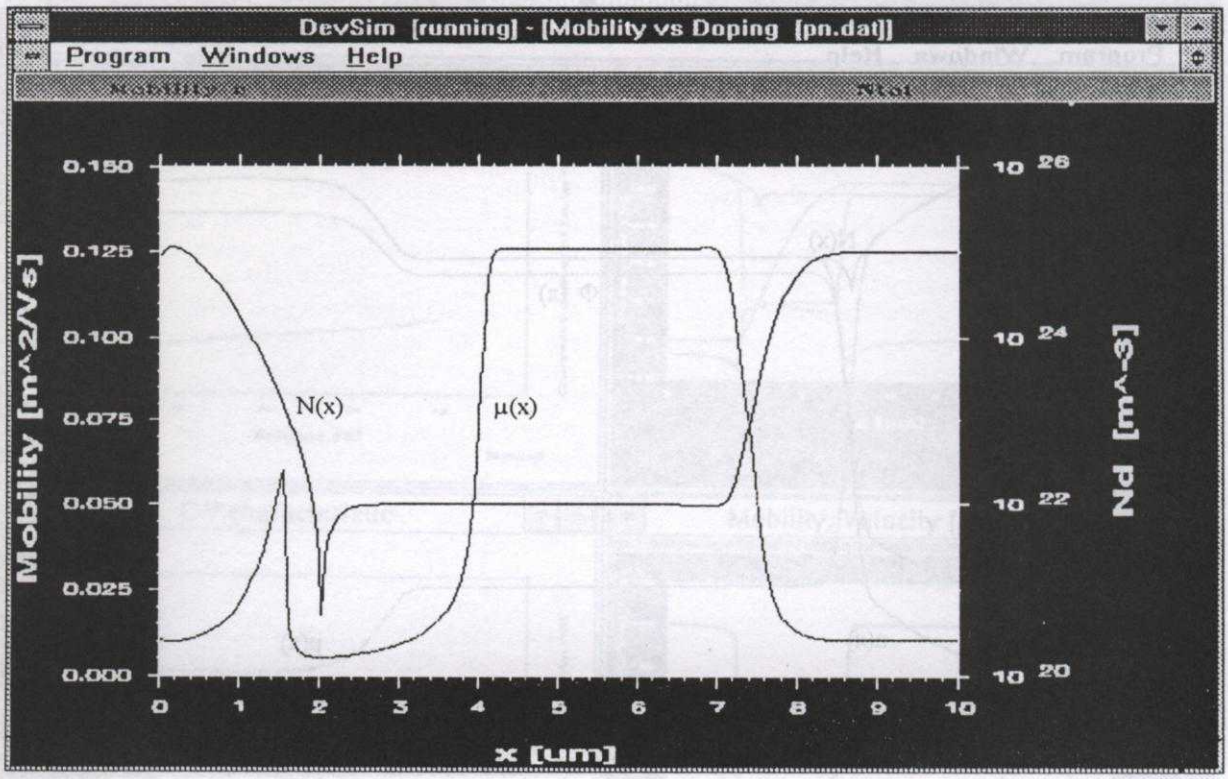


b)

Fig. 2. Free-carrier distributions, doping profile and distribution of electrostatic potential in thermal equilibrium (a) and at reverse voltage of $V_r = 40$ V (b).



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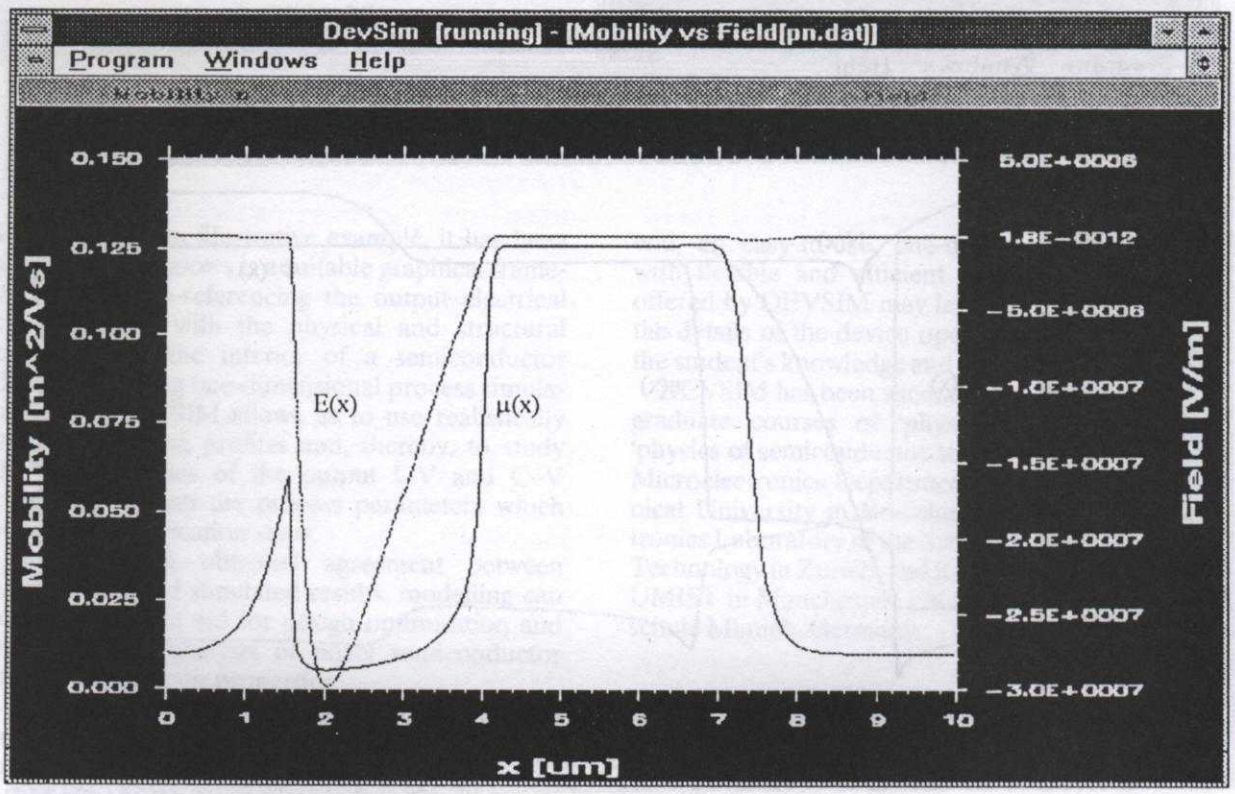
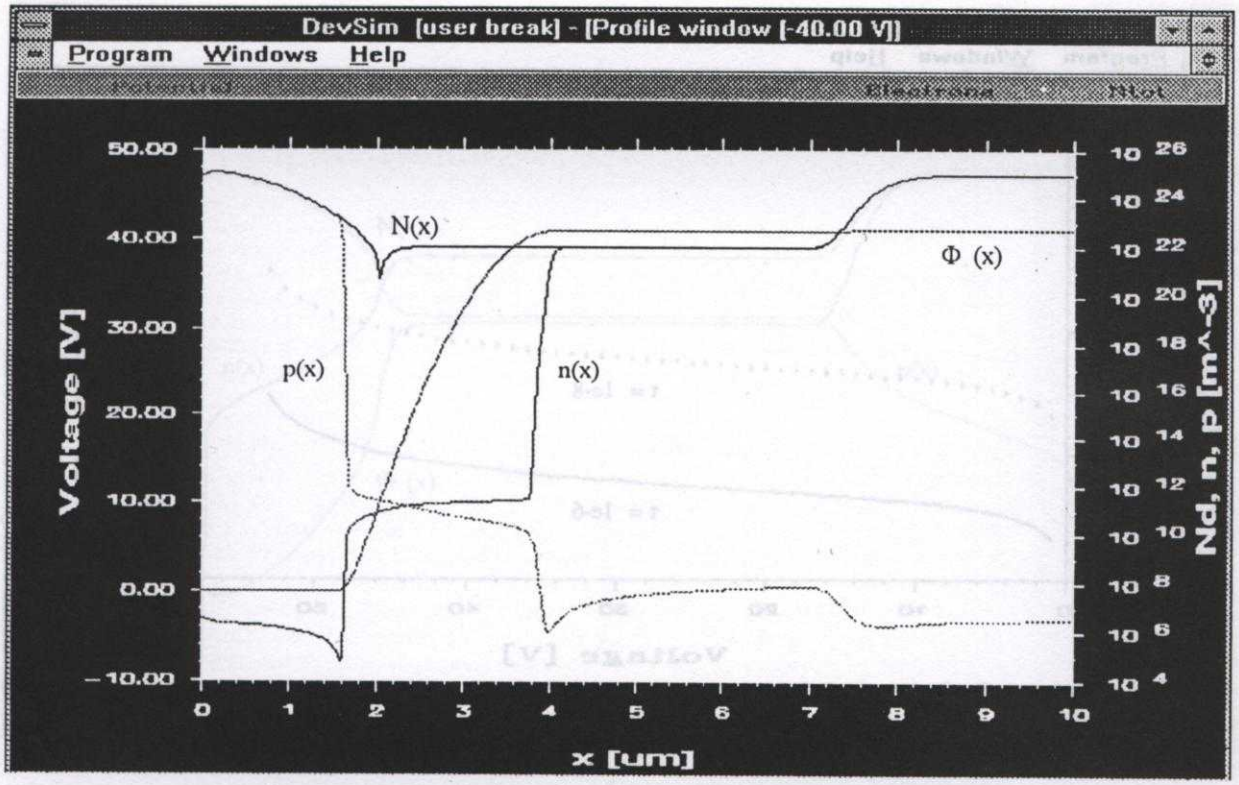


b)

Fig. 3. Dependence of the carrier mobility on net doping concentration (a) and on the electric field strength (b).



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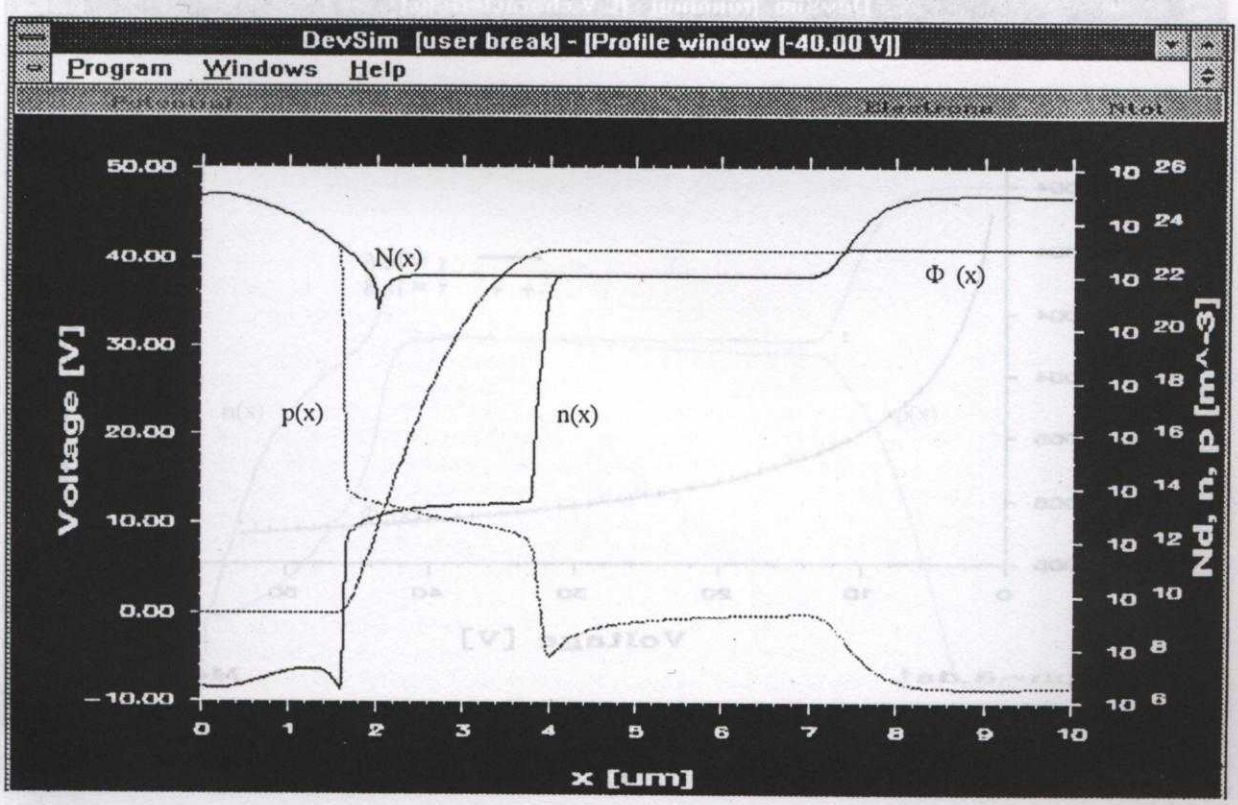
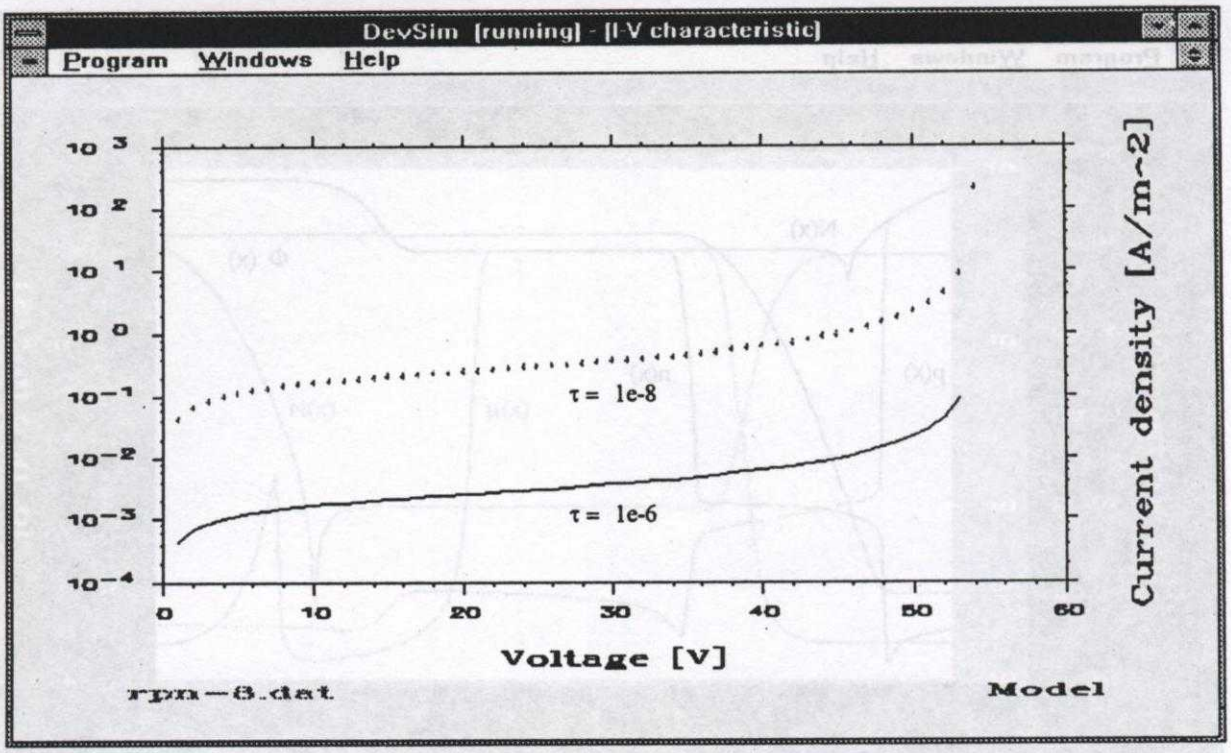


b)

Fig. 4. Distribution of electric potential and free-carrier concentration in the interior of the analysed structure at $V_r = 40$ V for $\tau = 10^{-6}$ s (a) and $\tau = 10^{-8}$ s (b).



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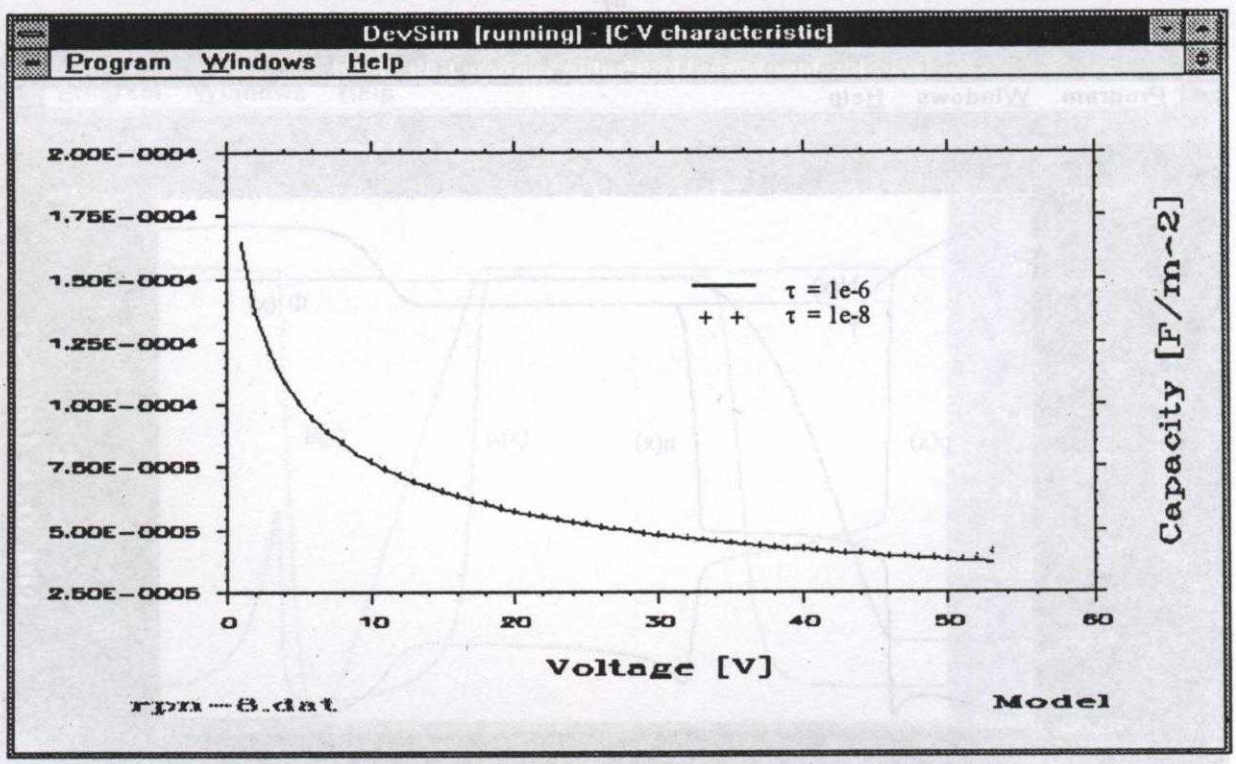

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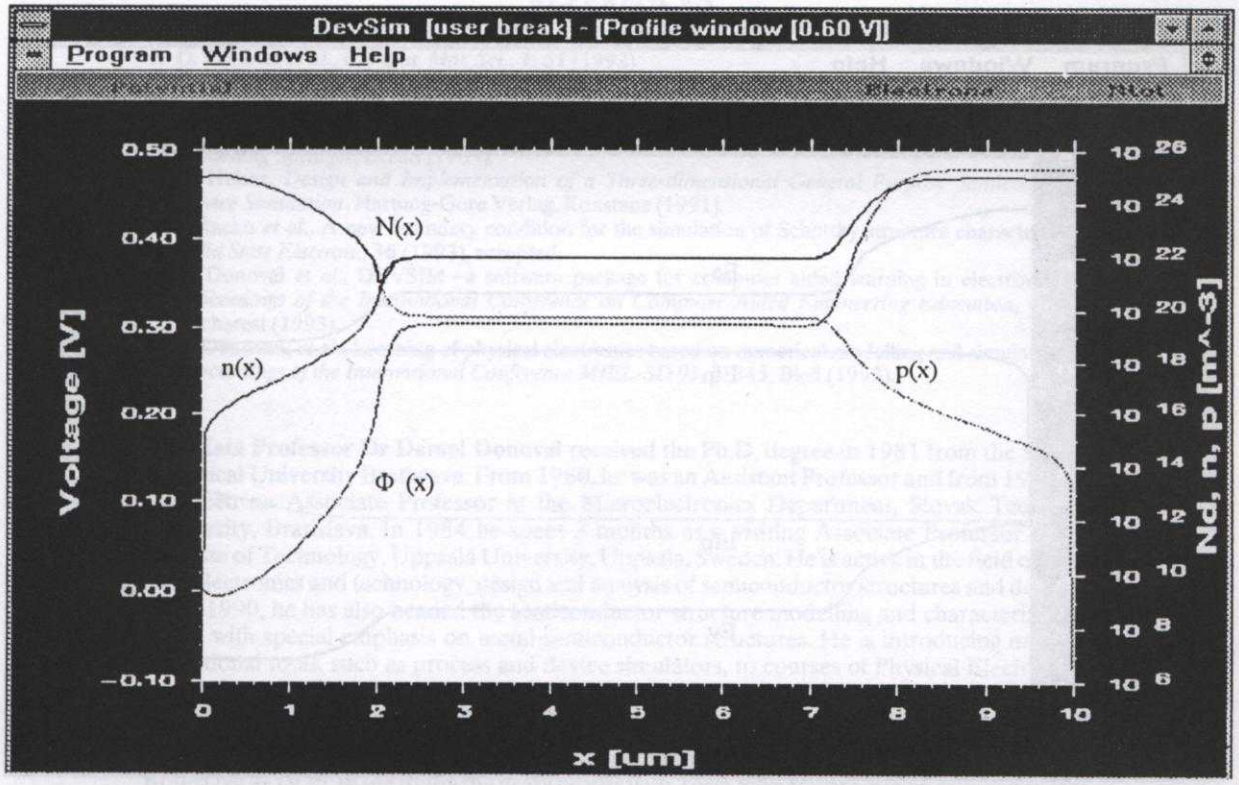
Fig. 5. Output I–V (a) and C–V (b) characteristics of the analysed structure for two different carrier lifetimes.



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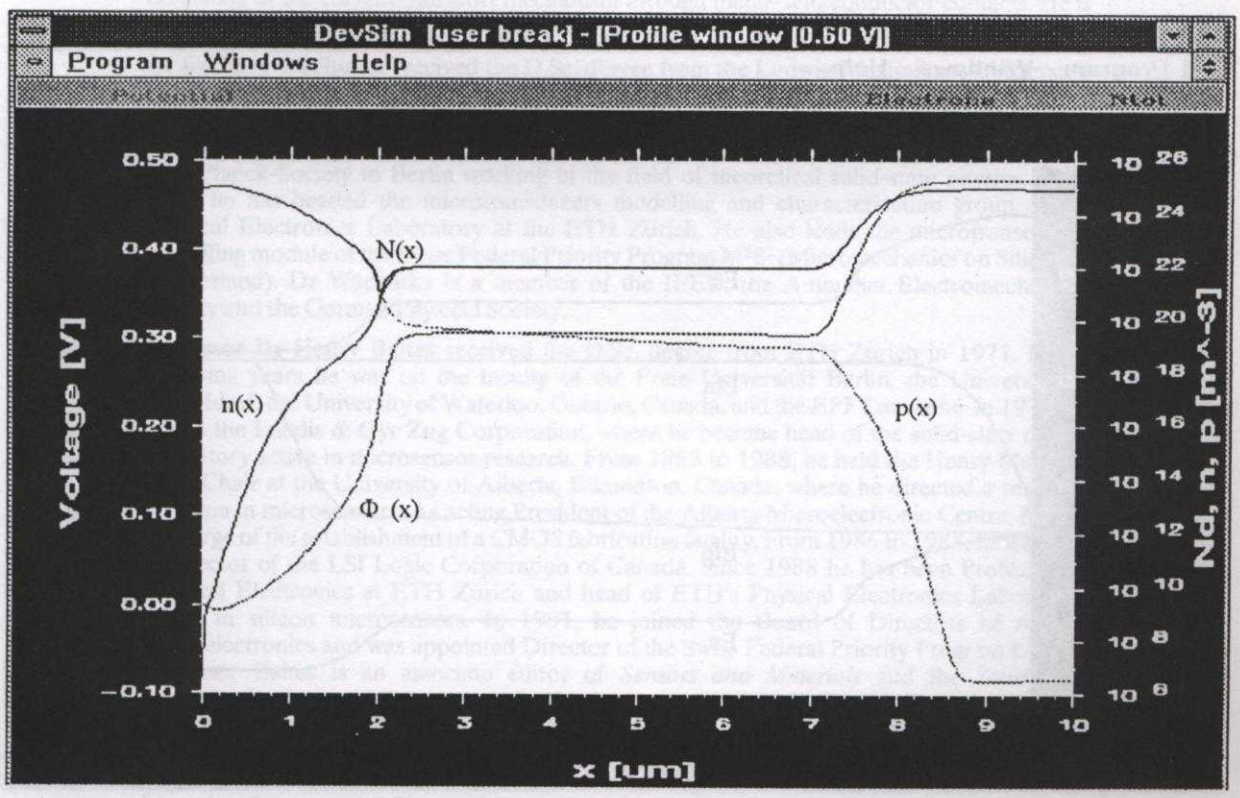
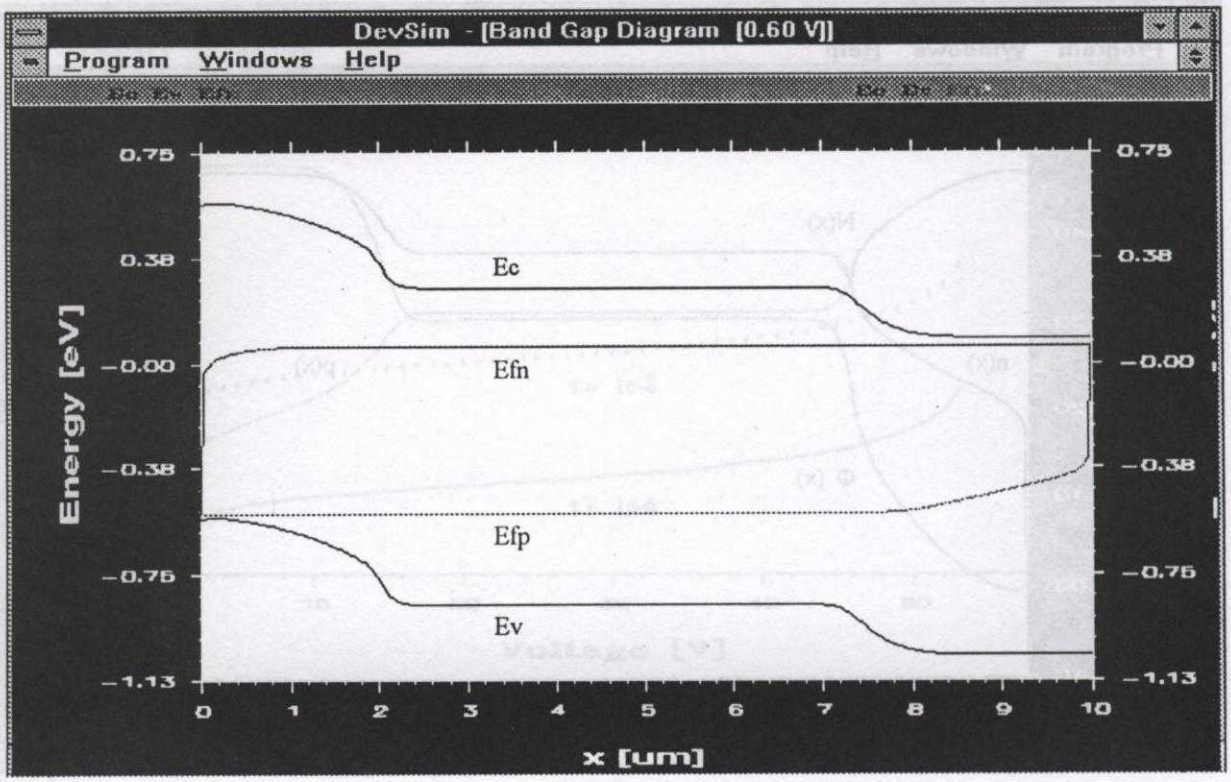


b)

Fig. 6. Distribution of electric potential and free carrier concentration in the interior of the analysed structure at $V_f = 0.40$ V for $\tau = 10^{-6}$ s (a) and $\tau = 10^{-8}$ s (b).



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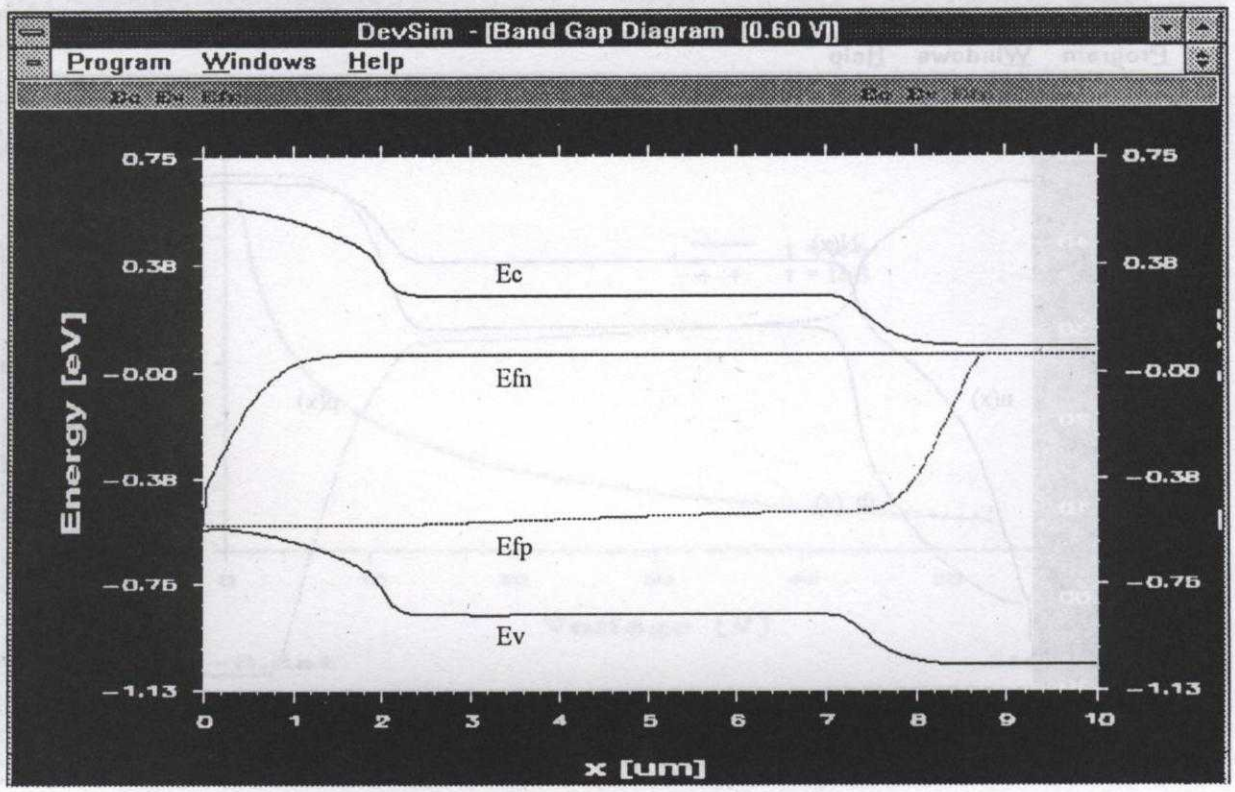

b)

Fig. 7. Energy band diagram of the analysed structure at $V_f = 0.40$ V for $\tau = 10^{-6}$ s (a) and $\tau = 10^{-8}$ s (b).

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